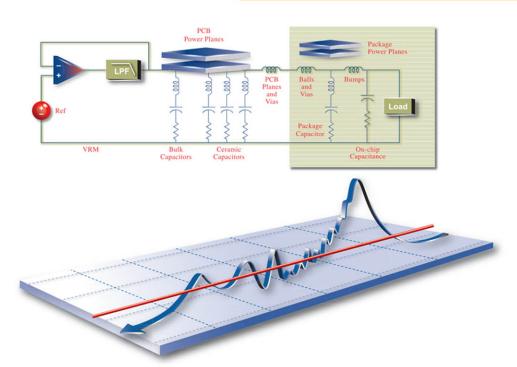


# Principles of Power Integrity for PDN Design

Robust and Cost Effective Design for High Speed Digital Products

### **SIMPLIFIED**



Larry D. Smith • Eric Bogatin

# PRINCIPLES OF POWER INTEGRITY FOR PDN DESIGN— SIMPLIFIED

# Principles of Power Integrity for PDN Design--Simplified: Robust and Cost Effective Design for High Speed Digital Products

#### **Table of Contents**

$\sim$	_		_	
	O	v	е	r

Title Page

Copyright Page

Contents

**Preface** 

Acknowledgments

About the Authors

Chapter 1 Engineering the Power Delivery Network

- 1.1 What Is the Power Delivery Network (PDN) and Why Should I Care?
- 1.2 Engineering the PDN
- 1.3 Working or Robust PDN Design
- 1.4 Sculpting the PDN Impedance Profile
- 1.5 The Bottom Line

Reference

Chapter 2 Essential Principles of Impedance for PDN Design

- 2.1 Why Do We Care About Impedance?
- 2.2 Impedance in the Frequency Domain
- 2.3 Calculating or Simulating Impedance



- 2.4 Real Circuit Components vs. Ideal Circuit Elements
- 2.5 The Series RLC Circuit
- 2.6 The Parallel RLC Circuit
- 2.7 The Resonant Properties of a Series and Parallel RLC Circuit
- 2.8 Examples of RLC Circuits and Real Capacitors
- 2.9 The PDN as Viewed by the Chip or by the Board
- 2.10 Transient Response
- 2.11 Advanced Topic: The Impedance Matrix
- 2.12 The Bottom Line

#### References

#### Chapter 3 Measuring Low Impedance

- 3.1 Why Do We Care About Measuring Low Impedance?
- 3.2 Measurements Based on the V/I Definition of Impedance
- 3.3 Measuring Impedance Based on the Reflection of Signals
- 3.4 Measuring Impedance with a VNA
- 3.5 Example: Measuring the Impedance of Two Leads in a DIP
- 3.6 Example: Measuring the Impedance of a Small Wire Loop
- 3.7 Limitations of VNA Impedance Measurements at Low Frequency
- 3.8 The Four-Point Kelvin Resistance Measurement Technique
- 3.9 The Two-Port Low Impedance Measurement Technique
- 3.10 Example: Measuring the Impedance of a 1-inch Diameter Copper Loop
- 3.11 Accounting for Fixture Artifacts
- 3.12 Example: Measured Inductance of a Via
- 3.13 Example: Small MLCC Capacitor on a Board
- 3.14 Advanced Topic: Measuring On-Die Capacitance
- 3.15 The Bottom Line



#### References

#### Chapter 4 Inductance and PDN Design

- 4.1 Why Do We Care About Inductance in PDN Design?
- 4.2 A Brief Review of Capacitance to Put Inductance in Perspective
- 4.3 What Is Inductance? Essential Principles of Magnetic Fields and Inductance
- 4.4 Impedance of an Inductor
- 4.5 The Quasi-Static Approximation for Inductance
- 4.6 Magnetic Field Density, B
- 4.7 Inductance and Energy in the Magnetic Field
- 4.8 Maxwells Equations and Loop Inductance
- 4.9 Internal and External Inductance and Skin Depth
- 4.10 Loop and Partial, Self- and Mutual Inductance
- 4.11 Uniform Round Conductors
- 4.12 Approximations for the Loop Inductance of Round Loops
- 4.13 Loop Inductance of Wide Conductors Close Together
- 4.14 Approximations for the Loop Inductance of Any Uniform Transmission Line
- 4.15 A Simple Rule of Thumb for Loop Inductance
- 4.16 Advanced Topic: Extracting Loop Inductance from the S-parameters Calculated with a 3D Field Solver
- 4.17 The Bottom Line

References

# Chapter 5 Practical Multi-Layer Ceramic Chip Capacitor Integration

- 5.1 Why Use Capacitors?
- 5.2 Equivalent Circuit Models for Real Capacitors



- 5.3 Combining Multiple Identical Capacitors in Parallel
- 5.4 The Parallel Resonance Frequency Between Two Different Capacitors
- 5.5 The Peak Impedance at the PRF
- 5.6 Engineering the Capacitance of a Capacitor
- 5.7 Capacitor Temperature and Voltage Stability
- 5.8 How Much Capacitance Is Enough?
- 5.9 The ESR of Real Capacitors: First- and Second-Order Models
- 5.10 Estimating the ESR of Capacitors from Spec Sheets
- 5.11 Controlled ESR Capacitors
- 5.12 Mounting Inductance of a Capacitor
- 5.13 Using Vendor-Supplied S-parameter Capacitor Models
- 5.14 How to Analyze Vendor-Supplied S-Parameter Models
- 5.15 Advanced Topics: A Higher Bandwidth Capacitor Model
- 5.16 The Bottom Line

References

#### Chapter 6 Properties of Planes and Capacitors

- 6.1 The Key Role of Planes
- 6.2 Low-Frequency Property of Planes: Parallel Plate Capacitance
- 6.3 Low-Frequency Property of Planes: Fringe Field Capacitance
- 6.4 Low-Frequency Property of Planes: Fringe Field Capacitance in Power Puddles
- 6.5 Loop Inductance of Long, Narrow Cavities
- 6.6 Spreading Inductance in Wide Cavities
- 6.7 Extracting Spreading Inductance from a 3D Field Solver
- 6.8 Lumped-Circuit Series and Parallel Self-Resonant Frequency



- 6.9 Exploring the Features of the Series LC Resonance
- 6.10 Spreading Inductance and Source Contact Location
- 6.11 Spreading Inductance Between Two Contact Points
- 6.12 The Interactions of a Capacitor and Cavities
- 6.13 The Role of Spreading Inductance: When Does Capacitor Location Matter?
- 6.14 Saturating the Spreading Inductance
- 6.15 Cavity Modal Resonances and Transmission Line Properties
- 6.16 Input Impedance of a Transmission Line and Modal Resonances
- 6.17 Modal Resonances and Attenuation
- 6.18 Cavity Modes in Two Dimensions
- 6.19 Advanced Topic: Using Transfer Impedance to Probe Spreading Inductance
- 6.20 The Bottom Line

References

## Chapter 7 Taming Signal Integrity Problems When Signals Change Return Planes

- 7.1 Signal Integrity and Planes
- 7.2 Why the Peak Impedances Matter
- 7.3 Reducing Cavity Noise through Lower Impedance and Higher Damping
- 7.4 Suppressing Cavity Resonances with Shorting Vias
- 7.5 Suppressing Cavity Resonances with Many DC Blocking Capacitors
- 7.6 Estimating the Number of DC Blocking Capacitors to Suppress Cavity Resonances



- 7.7 Determining How Many DC Blocking Capacitors Are Needed to Carry Return Current
- 7.8 Cavity Impedance with a Suboptimal Number of DC Blocking Capacitors
- 7.9 Spreading Inductance and Capacitor Mounting Inductance
- 7.10 Using Damping to Suppress Parallel Resonant Peaks Created by a Few Capacitors
- 7.11 Cavity Losses and Impedance Peak Reduction
- 7.12 Using Multiple Capacitor Values to Suppress Impedance Peak
- 7.13 Using Controlled ESR Capacitors to Reduce Peak Impedance
  Heights
- 7.14 Summary of the Most Important Design Principles for Managing Return Planes
- 7.15 Advanced Topic: Modeling Planes with Transmission Line Circuits
- 7.16 The Bottom Line

References

#### Chapter 8 The PDN Ecology

- 8.1 Putting the Elements Together: The PDN Ecology and the Frequency Domain
- 8.2 At the High-Frequency End: The On-Die Decoupling Capacitance
- 8.3 The Package PDN
- 8.4 The Bandini Mountain
- 8.5 Estimating the Typical Bandini Mountain Frequency
- 8.6 Intrinsic Damping of the Bandini Mountain
- 8.7 The Power Ground Planes with Multiple Via Pair Contacts



- 8.8 Looking from the Chip Through the Package into the PCB Cavity
- 8.9 Role of the Cavity: Small Boards, Large Boards, and Power Puddles
- 8.10 At the Low Frequency: The VRM and Its Bulk Capacitor
- 8.11 Bulk Capacitors: How Much Capacitance Is Enough?
- 8.12 Optimizing the Bulk Capacitor and VRM
- 8.13 Building the PDN Ecosystem: The VRM, Bulk Capacitor, Cavity, Package, and On-Die Capacitance
- 8.14 The Fundamental Limits to the Peak Impedance
- 8.15 Using One Value MLCC Capacitor on the Board-General Features
- 8.16 Optimizing the Single MLCC Capacitance Value
- 8.17 Using Three Different Values of MLCC Capacitors on the Board
- 8.18 Optimizing the Values of Three Capacitors
- 8.19 The Frequency Domain Target Impedance Method (FDTIM) for Selecting Capacitor Values and the Minimum Number of Capacitors
- 8.20 Selecting Capacitor Values with the FDTIM
- 8.21 When the On-Die Capacitance Is Large and Package Lead Inductance Is Small
- 8.22 An Alternative Decoupling Strategy Using Controlled ESR Capacitors
- 8.23 On-Package Decoupling (OPD) Capacitors
- 8.24 Advanced Section: Impact of Multiple Chips on the Board Sharing the Same Rail
- 8.25 The Bottom Line



#### References

#### Chapter 9 Transient Currents and PDN Voltage Noise

- 9.1 Whats So Important About the Transient Current?
- 9.2 A Flat Impedance Profile, a Transient Current, and a Target Impedance
- 9.3 Estimating the Transient Current to Calculate the Target Impedance with a Flat Impedance Profile
- 9.4 The Actual PDN Current Profile Through a Die
- 9.5 Clock-Edge Current When Capacitance Is Referenced to Both Vss and Vdd
- 9.6 Measurement Example: Embedded Controller Processor
- 9.7 The Real Origin of PDN NoiseHow Clock-Edge Current Drives PDN Noise
- 9.8 Equations That Govern a PDN Impedance Peak
- 9.9 The Most Important Current Waveforms That Characterize the PDN
- 9.10 PDN Response to an Impulse of Dynamic Current
- 9.11 PDN Response to a Step Change in Dynamic Current
- 9.12 PDN Response to a Square Wave of Dynamic Current at Resonance
- 9.13 Target Impedance and the Transient and AC Steady-State Responses
- 9.14 Impact of Reactive Elements, q-Factor, and Peak Impedances on PDN Voltage Noise
- 9.15 Roque Waves
- 9.16 A Robust Design Strategy in the Presence of Rogue Waves
- 9.17 Clock-Edge Current Impulses from Switched Capacitor Loads



- 9.18 Transient Current Waveforms Composed of a Series of Clock Impulses
- 9.19 Advanced Section: Applying Clock Gating, Clock Swallowing, and Power Gating to Real CMOS Situations
- 9.20 Advanced Section: Power Gating
- 9.21 The Bottom Line

References

## Chapter 10 Putting It All Together: A Practical Approach to PDN Design

- 10.1 Reiterating Our Goal in PDN Design
- 10.2 Summary of the Most Important Power Integrity Principles
- 10.3 Introducing a Spreadsheet to Explore Design Space
- 10.4 Lines 112: PDN Input Voltage, Current, and Target Impedance Parameters
- 10.5 Lines 1324: 0th Dip (Clock-Edge) Noise and On-Die Parameters
- 10.6 Extracting the Mounting Inductance and Resistance
- 10.7 Analyzing Typical Board and Package Geometries for Inductance
- 10.8 The Three Loops of the PDN Resonance Calculator (PRC)
  Spreadsheet
- 10.9 The Performance Figures of Merit
- 10.10 Significance of Damping and q-factors
- 10.11 Using a Switched Capacitor Load Model to Stimulate the PDN
- 10.12 Impulse, Step, and Resonance Response for Three-Peak PDN: Correlation to Transient Simulation



- 10.13 Individual q-factors in Both the Frequency and Time Domains
- 10.14 Rise Time and Stimulation of Impedance Peak
- 10.15 Improvements for a Three-Peak PDN: Reduced Loop
  Inductance of the Bandini Mountain and Selective MLCC Capacitor
  Values
- 10.16 Improvements for a Three-Peak PDN: A Better SMPS Model
- 10.17 Improvements for a Three-Peak PDN: On-Package Decoupling (OPD) Capacitors
- 10.18 Transient Response of the PDN: Before and After Improvement
- 10.19 Re-examining Transient Current Assumptions
- 10.20 Practical Limitations: Risk, Performance, and Cost Tradeoffs
- 10.21 Reverse Engineering the PDN Features from Measurements
- 10.22 Simulation-to-Measurement Correlation
- 10.23 Summary of the Simulated and Measured PDN Impedance and Voltage Features
- 10.24 The Bottom Line

References

Index

