shortcut

The Design for Trustworthy Software Compilation

Taguchi Methods and Optimization for Robust Software

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This article is an adaptation of Chapter 17 from the book *Design for Trustworthy Software* by Bijay K. Jayaswal and Peter C. Patton (0-13-187250-8, Prentice Hall).

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for trustworthiness in use. Hence, we will not repeat or even summarize the vast literature on the successful application of Taguchi Methods in manufacturing, but rather focus on their application to the design of robust software.

TABLE 1   Steps in Taguchi Methods

Step Number	Step	Description
1	Define the problem.	Clearly state the problem to be solved.
2	Determine the objective.	Identify performance responses to be optimized.
3	Brainstorm.	Identify both signal and noise factors.
4	Design the experiment.	Choose factors and build orthogonal arrays.
5	Conduct the experiment.	Perform trials and collect data.
6	Analyze the data.	Evaluate TMP and NPM for each trial run.
7	Interpret the results.	Identify variability and target control factors and select their optima.
8	Confirm the experiment.	Prove that new parameter settings enhance robustness.

An Example from Engineering Design

Although our interest here is software design, a simpler yet realistic example from electrical circuit design may be very helpful in giving you insight into Taguchi Methods. This application shows the trade-off potential between the three stages of Taguchi design and also gives you insight into the increasing replacement of electronic circuits by software algorithms. Analog filters for radio and other signal processing have long since been replaced by digital (software-programmed) filters. Modern communication receivers are simply computer programs that tune to and receive signals on a chip-based computer. Similarly, the most advanced radio transmitters are computers that, rather than computing a number, prepare and transmit a signal at a chosen or preprogrammed frequency. As an example, we take a case study from the literature by Kanemoto.[4]

Much of electrical circuit design involves adjusting part values and their tolerances to achieve a target perform-ance over a certain range with the minimum number of parts and the least constraint on part tolerances. Normally, electronic components have tolerance values of

plus or minus 20 percent. High-quality parts with a 10 percent tolerance are very expensive. Parts having 1 percent tolerance are even more expensive and usually are reserved for laboratory or standards use. Figure 3a shows a simple frequency-modulated oscillator consisting of an inverter, a piezoelectric crystal, two resistors, two capacitors, and two voltage-dependent variable capacitors. Figure 3b shows the voltage variation resulting from a modulation signal V around a 2V dc bias value. Figure 3c shows the frequency deviation resulting from the signal voltage. Clearly the performance value of this circuit is to maintain a relationship between frequency deviation (output) and a varying signal voltage (input). This performance target can be disturbed by noise factors such as environmental temperature, time drift, and power fluctuation, but the latter is the principal noise factor, ranging from +/–0.5V. When designing an electronic circuit, it is simple enough to bench-test it to determine variation around the target value of zero deviation from a center frequency of 453.286 kHz for an input signal voltage of 0. In this case, you can do a full factorial study, since there are so few parameters.
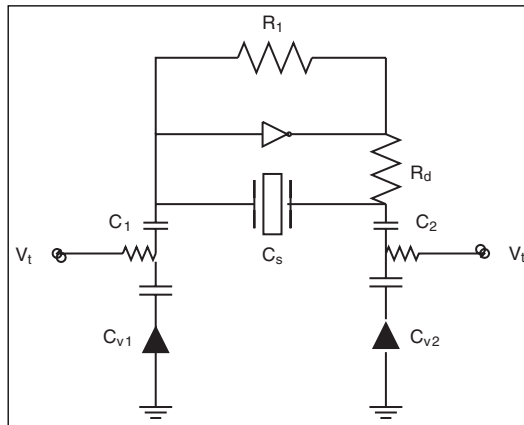

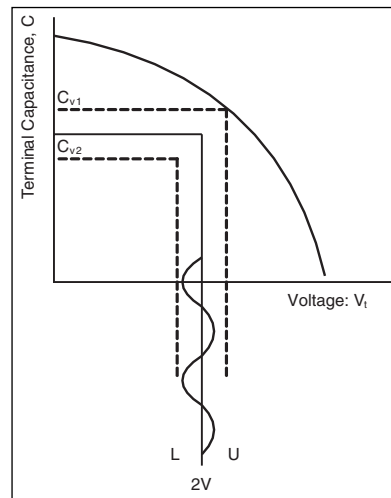FIGURE 3A   Frequency-Modulated Oscillator: The Experimental Circuit
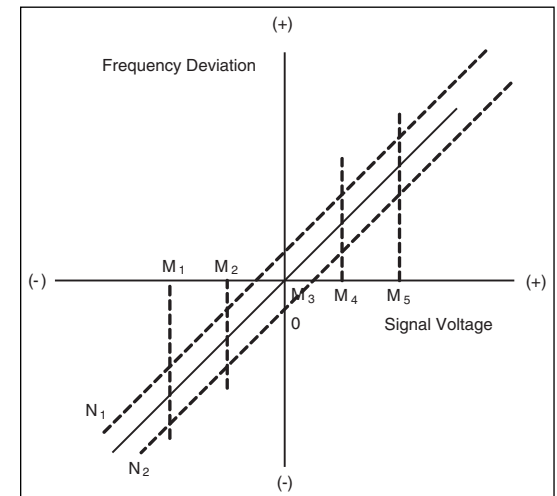

FIGURE 3B   Voltage Variation

FIGURE 3C   Frequency Deviation

An Example from Engineering Design

The experiments with Kanemoto's circuit showed an error variation of 12.763 Hz and an error variance of 1596. The control factors and their levels are shown in Table 2, in which power source voltage is the voltage input to the inverter. This data is put into an orthogonal array to carry out the statistical experiment. The results are shown in Table 3. It gives the SNR and sensitivity values for the original configuration, the optimal configuration, and the improvement or gain, along with the results of the follow-up confirmatory experiment. The factors for the original circuit are $A_1B_2C_2D_2E_2F_2H_2$—that is, the first crystal choice, a CSB-455 in column 1 of the factor table, and the

second, or column 2, choice for all the other factors. The optimal circuit given these factors and the single-noise factor of the small power supply voltage instability is $A_2B_3C_3D_3E_3F_2G_2H_3$. This would be the circuit with the second crystal choice, a B456-F15, R1 = 1 kOhm, Rd = 5.6 kOhms, C2 = C1 = 820 mfd, and both capacitors of chip type, and the bias on the inverter set at 7 volts. This is a rather simple problem, but it does show Taguchi Methods favorably. You can vary all the factors at once to optimize the circuit in one statistical experiment and its confirmation, rather than fiddling at the designer's bench for days or doing hundreds of circuit simulations, changing one part value at a time.

TABLE 2 Circuit Control Factors and Levels

Label	Control Factor Name	Level 1	Level 2	Level 3
A	Crystal type	Type A	Type B	Type C
B	Resistor R1	680 Ohms	820 Ohms	1 kOhm
C	Resistor Rd	3.3 kOhm	4.7 kOhm	5.6 kOhm
D	Capacitor C1	560 mfd	680 mfd	820 mfd
E	Capacitor C2	Two levels below C1	One level below C1	Same as C1
F	Capacitor type	Ceramic	Chip	Film
G	Capacitor type	Ceramic	Chip	Film
H	Power source voltage	3	5	7